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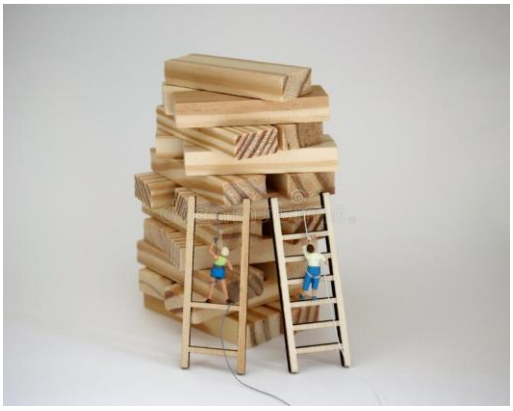
Excelli*focus*

Addressing the challenges of the RTL & Implementation Teams in Closing Timing & Realizing a Robust Design on Schedule with High Confidence

In this issue we look at the challenges involved transition from design to implementation and how to modernize the traditional ASIC flows



Modernizing ASIC Design Process

Brief overview of challenges and issues faced by design and implementation teams

Building chips is a daunting task and full of challenges. Designs are getting larger, geometries are shrinking and we keep packing more and more into smaller and smaller area while we have to make sure power consumption is minimized, timing is optimized and much more. Such product requirements manifest itself in design from planning to partitioning the design, and designing logic and clock networks which address the end goal.

Traditional methods are continuously updated to address such challenges and from time to time there is a need for disruptive changes in order to cover the gaps of traditional methods. We witnessed such disruptive changes with advent of synthesis, later Assertion based verification, and later LEC; logical equivalency checking. No one can imagine designing chip these days without them.

Today the we are witnessing similar types of bottlenecks when it comes to floor planning, timing constraints, Clock and reset distribution, statis and dynamic verification, etc. which are for the most part done There is little automation and any available tools are simply band-aids to keep the conveyor belt moving. The result are more risk and uncertainty, more design fails, and many iterations.

The need for automation is becoming more and more apparent as design geometries are shrinking, power requirements are becoming more stringent. Some point tools have become part of mainstream design flow such as Clock Domain Crossing; CDC, analysis, but they still require much manual intervention and setup. We are making incremental changes but nothing disruptive yet to address the challenges.

For example, much of design planning is done on back of envelops and scratch papers trying to address, area, power through portioning the design for optimal timing closure, not much automation is involved. One has to consider the impact of data connectivity, congestion, power planning, abutment issues and more.

This leads to further challenges when it comes down to clock and reset distribution and planning for it ahead of time with 1000's of functionality of such design is a challenge which is not easy to address using current CDC, ABV, or formal methods. Even emulation adds another layer of complexity to the equation which requires a team of experts at a great cost in time and capital. On the timing side Constraints development is pretty much manual with a sprinkle of excel sheet automation, and some band-aid checkers while designers need a way to quickly have high quality constraints for CTS, Synthesis, P&R, or CDC for various modes for each one of the blocks and sub components. This challenge becomes even more tedious when we are trying to do such design and verification for various modes, such as functional, low power, or test across multiple blocks on a chip. Later in the implementation phase the verification challenges become unmanageable for the massive number of structures implemented on the chip, to the point of not being viable and providing diminishing returns. As an example, Gate Level Simulation becomes unrealistic from practicality stand point, and the question is that if it is even needed or how it can broken up in a meaningful way.

If we look at the origins of these problems much of it starts at the transition from design realization to implementation when many new variables are

manually and with use of archaic tools such as spreadsheets.

clocks spanning the entire modern design. Once implemented the verification of timing and

introduced to the process. This is where automation can help to manage the complexity and sheer volume of data. As an example, an intelligent budgeting can help in determining the proper partitioning of the design during or even before the floor plans are defined, and further help in more efficient clocking, resulting in reduced number of potential issues which may slip from various checking tools. This type of automation can address the issues before they become issues.

Transition from a working and well tested methodology is always a risky move and inevitably involves much work to make changes. However, the alternative is to continue with so called "proven" methods at the expense of increased risk and more work downstream. Automation can eliminate the iterations, can provide much more insight into the process and allow for processing of much larger amount of data in order to streamline the existing methodologies.

AUTOMOTIVE REQUIREMENTS

As automotive manufacturers make cars and tucks smarter and more interactive, chips are becoming an integral part of the automotive design. Up until recently the chips controlled small and relatively simple components in the car such as ignitions, ventilation system, and for the most part limited to very specific tasks on the car. A chip failure meant a replacement of components in the event of a recall or repair.

In the past few years, the cars have gone from a mechanical component to more of an electronic processing centers with massive compute power and ability to not only interact with the communication towers but also make autonomous decisions interacting with the surrounding environment just like a human being does. Automated driving and self-parking cars are some examples of these innovations. Innovations are essential to our progress in chip business; however, the cost of this innovation often involves risks and safety measures.

The chip industry was not driven by manufacturing standards in the past, much of the standards were self-imposed for the

electronics, essential to operation of the vehicle are being integrated into these products.

ISO-26262 is an example of such standard being required by automotive manufacturers to mitigate failure risks and reduce the chip products quality issues which may impact safety and viability of electronics in today's vehicles. Component manufacturers have been adhering to ISO standards for many years, now the chip makers are also being required to adhere to these standards in every step of their design process as the safety of such components is directly linked to quality of chip design. This requirement is also trickling down to tool providers who are directly involved in design and production of chips. EDA is now more and more involved in design of chips and the methodologies implemented for chip design often have a series of tools linked together for completion of the design. Designers, required by Automotive industry, are now responsible to ensure their designs are meeting minimum ISO-26262 requirements.

As a design team involved in automotive industry one must consider adherence to ISO-26262 standards and follow the methodologies

purpose of higher capacity and lower business risk and consistence and interoperability. What is the worst thing that can happen if a modem or a set top box fails?

The automotive industry is a different beast in that regard. There are many regulations involved, and better or worst they are designed to protect lives and impose some minimum requirements for safety. ISO standards have been part of manufacturing processes for many decades, and now they are starting to expand into the chip industry as more and more

and practices defined by the standard. Also, expect these requirements to become part of other areas of Chip making and EDA as more of electronics are integrated into automotive products.

SOC Clocking & Reset Challenge

In the next issue we explore the challenges and techniques addressing the Clocking and Reset involved in design of today's chip and how to bring automation to the mix to address such challenges.

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