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IP Timing Constraints Promotion Challenges

A method to automatically generate SoC Timing Constraints

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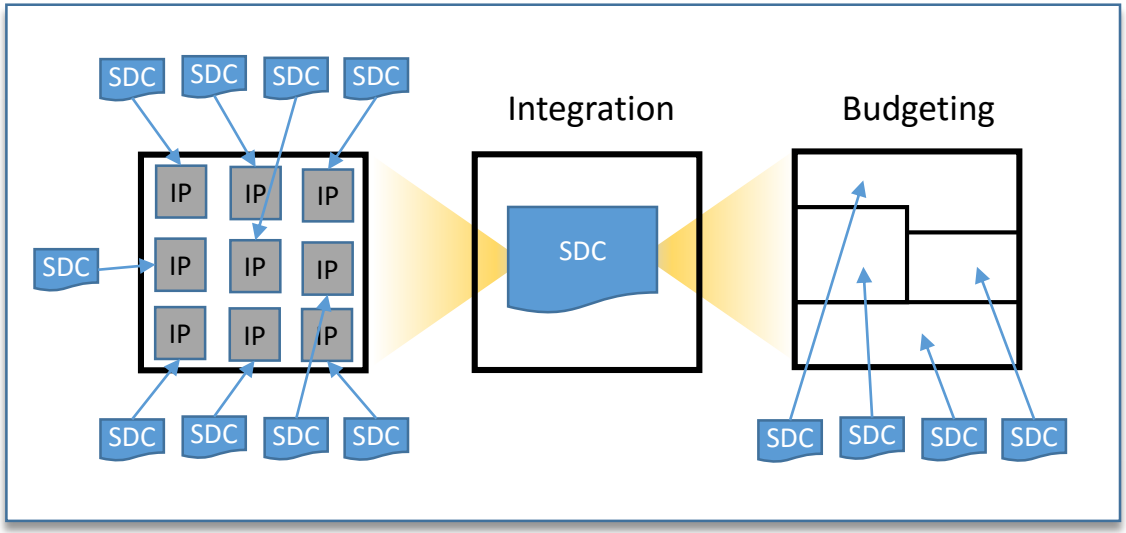
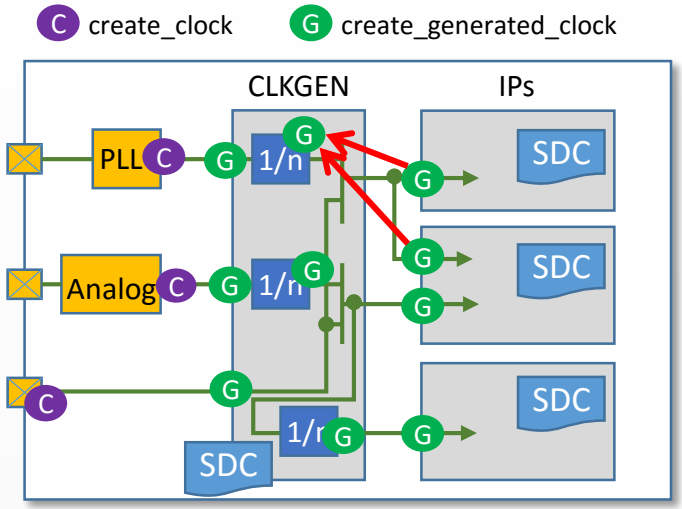
Motivation





- Today's SoC contain large amount of external or internal IP's. Each IP has its own timing constraints.

- Integration if IP constraints poses a challenge because
  - The timing designer must first understand the IP clocking which is extremely hard if it's a 3rd party IP.
  - Manually connecting thousands of clocks between blocks in order to stitch the top level SDC is error prone, takes a long time and is very painful.

- Up until now, the SDC integration task had been mostly manual and time consuming operation with limited or no solution available from existing EDA vendors.
    - Depending on the design size, on average it takes about 8 Man-Months for the integration activities
    - It takes another 3.5 Man-Months for qualifying the correctness of the SDC

This paper presents a method of integrating and promotion of timing constraints using Excellicon's tools in order to significantly reduce the integration TAT and to generate a sign-off quality SDC

Objective

- Automatic discovery of all clocks in the design
  - This will help in alleviating the manual identification and writing of all clocks
- Display the clocking structure intuitively
  - Designers can easily understand the clock network and correct any issues early on
- Promotion & Demotion of IP constraints across the SoC
  - Provide guidance when constraints conflicts occurs
- Preserve the timing intent of the IP
  - After promotion, the IP SDC constraints should still reflect the original timing intent of the IP's since the IP owner guarantees correct operation of IP as long as the corresponding SDC is used
- Transform IP exceptions to Chip level
  - Boundary exceptions must be handled appropriately
- Reduce the integration TAT

Idea – Promotion with IP Isolation

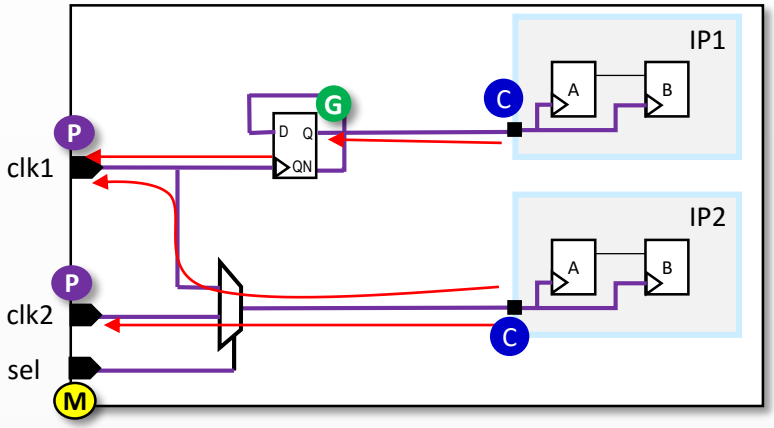
C IP SDC - *create_clock*

G Extracted - *create_generated_clock*

G Promoted SDC - *create_generated_clock*

P Extracted - *create_clock*

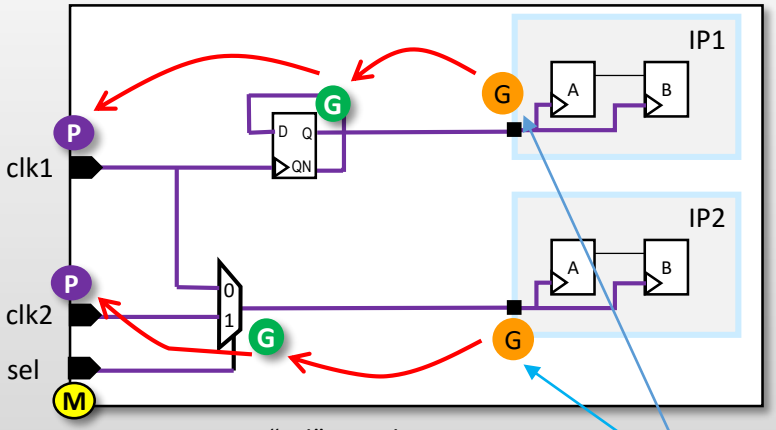
M Extracted – Mode Pin (control signal)



Clock extraction path shown in Red arrows

STEP1

- ❑ Extract clocks from where the *create_clock* is defined in the IP SDC
- ❑ If no SDC, extract clocks from the clock pin of the sequential cells
- ❑ Automatically identify and classify clocks from the control signals



"sel" signal set to 1

The *create_clock* replaced by *create_generated_clock* and "mastered" to the top level extracted G clock in promoted SDC

STEP2

- ❑ Replace IP *create_clock* with the *create_generated_clock*
- ❑ Promote the clock properties like freq, duty cycle to the top
- ❑ Promote other constraints like FP and MCPs
- ❑ Identify and create master relationship for each clock (shown in red arrows)
- ❑ Generate all other constraints like set_clock_groups, exceptions, IO delays etc.

Evidence

- We worked with Excellicon ConMan tool and implemented this feature
- Promoted results were verified by running 3rd party SDC equivalence tool

Size of Design = 50M Instances
Number of Clocks = 958

	Without ConMan	With ConMan
Clock Discovery + Promotion	1M Month	4 M Hours
Demotion	NA	NA

Size of Design = 500M Instances
Number of Clocks = 1389

	Without ConMan	With ConMan
Clock Discovery	1 M Month	0.1 M Month
Promotion	7 M Month	2 M Month
Demotion	0.25M Month (through PT)	0.25 M Month

Summary

- Excellicon's ConMan tool greatly simplified our flow and improved significantly the TAT
  - Integrated flow reduced many man hours of debug and analysis
- IP timing intent was 100% preserved with this method of promotion
- Abstract clock visualization helped in pruning out early clock network issues
  - Helped in understanding the clocking network
- Better Quality of SDC than before
  - Eliminated iteration cycles that occurred with the manual method
- Eliminated ambiguity between design teams which eased the handoff issues
  - Using the single database to pass timing data between the design teams
- Single database from which SDC's can be generated for any hierarchy and for any mode